## IN THE CLAIMS

Please amend the claims as follows.

1. (Previously presented) A microelectronic package, comprising:

a microelectronic die having an active surface and at least one side;

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

2. (Previously Presented) The microelectronic package of claim 1, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

3. (Previously Presented) The microelectronic package of claim 2, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

4. (Original) The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

Claims 5-23. (Canceled)

24. (Previously Presented) The microelectronic package of claim 4, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

25. (Previously Presented) The microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die.

26. (Previously Presented) A microelectronic package, comprising:

a microelectronic die having an active surface, a back surface, and at least one side; and

encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface.

27. (Previously Presented) The microelectronic package of claim 26, further including at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

28. (Previously Presented) The microelectronic package of claim 27, further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

29. (Previously Presented) The microelectronic package of claim 28, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

30. (Previously Presented) The microelectronic package of claim 26, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

31. (Currently amended) A microelectronic package, comprising:

a plurality of microelectronic dice each having an active surface and at least one side; [[and]]

encapsulation material adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one surface substantially planar to said plurality of microelectronic dice active surfaces; and

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

32. (Canceled)

33. (Currently amended) The microelectronic package of claim 31 [[32]], further including at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer.

34. (Previously Presented) The microelectronic package of claim 33, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

35. (Previously Presented) The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

36. (Previously Presented) The microelectronic package of claim 35, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.

37. (Previously Presented) The microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die active surface.

38. (Previously Presented) A microelectronic package, comprising:

a microelectronic die having an active surface, a back surface, and at least one side; encapsulation material adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface;

a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface;

at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface; and

at least one heat dissipation device in thermal contact with said microelectronic die back surface.

39. (Previously Presented) The microelectronic package of claim 38, further including:

at least one second dielectric material layer disposed over said at least one first conductive trace and said first dielectric material layer, wherein at least a portion of at least one second conductive trace extends through and resides on said at least one second dielectric material layer.

40. (Previously Presented) The microelectronic package of claim 39, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device.